

BUR919990197US1

Sub  
Eq  
Cont

b) patterning the layer of germanium to form a germanium hard mask, the step further comprising:

- i) depositing a photo resist layer over the metallic germanium layer;
- ii) exposing and developing the photo resist layer to form a photolithography image;
- iii) etching the metallic germanium layer through the photolithography image; and
- iv) removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask;

Dio  
Cont.

c) patterning the dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the dielectric layer; and

further comprising the step of stripping away the germanium hard mask after patterning the dielectric layer, the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and removing the layer of germanium oxide.

---

REMARKS

09/599,783

9

BUR919990197US1

Claims 1, 2, 9, 10, 15-18, 24, 25 and 31 have been cancelled, as to reduce the number of claims for consideration. Further, claims 3-6, 8, 11, 12, 14, 19-21, 26, 28, 30 and 32 have been amended to better highlight the invention. In view of the amendments made and the following remarks, reconsideration of the present application is respectfully asked.

Claims 3, 4, 11, 19, 20, 26 and 27 have been objected to as being dependent upon a rejected base claim, but with the Examiner indicating that they would be allowable if rewritten in independent form. It is respectfully submitted that the above amendments place these claims in allowable form. In addition, changes have been made in claim dependencies so that all the claims remaining in the application, i.e. claims 3-6, 8, 11, 12, 14, 19-21, 26-28, 30 and 32, should be in condition for allowance.

Further, in view of the above claim cancellations and amendments, the remaining rejections should be rendered moot.

Accordingly, none of the references cited by the Examiner nor any other known prior art, either alone or in combination, disclose the unique combination of features disclosed in Applicants' claims presently on file. For this reason, allowance of all of Applicants' claims is respectfully solicited.

If any fees, including extension of time fees or additional claims fees, are due as a result of this response, please charge Deposit Account No. 09-0456. This authorization is intended to act as a constructive petition for an extension of time, should an extension of time be needed as a result of this response. The Examiner is invited to telephone the undersigned if this would in any

09/599,783

10

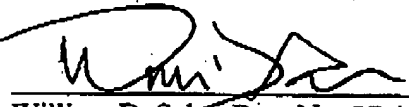
BUR919990197US1

way advance the prosecution of this case.

Respectfully submitted,

FOR: Furukawa, et al

BY:

  
\_\_\_\_\_  
William D. Sabo, Reg. No. 27,465  
IBM Corporation  
1000 River Street, 972E  
Essex Junction, Vt 05452  
Telephone: (802)769-9454

Dated: October 25, 2002

09/599,783

11

BUR919990197US1

**ATTACHMENT: VERSION WITH MARKINGS TO SHOW CHANGES MADE  
IN THE CLAIMS:**

3. (Amended) [The] A method [as claimed in claim 2] for etching a semiconductor substrate using a germanium hard mask, the semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of metallic germanium over the dielectric layer;

b) patterning the layer of metallic germanium to form the germanium hard mask as a top most layer over the dielectric layer, the step further comprising:

i) depositing a photo resist layer over the layer of metallic germanium;

ii) exposing and developing the photo resist layer to form a photolithography image;

iii) etching the layer of metallic germanium through the photolithography image;

and

iv) removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask;

c) selectively etching the dielectric layer through the germanium hard mask with the germanium hard mask as a top most layer to form an opening in the dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the dielectric layer; and

further comprising the step of stripping away the layer of metallic germanium after

09/599,783

12

BUR919990197US1

performing the step of selectively etching the dielectric layer, the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and  
removing the layer of germanium oxide.

4. (Amended) The method as claimed in claim 3, the step of removing the layer of germanium oxide including [rising] rinsing the semiconductor substrate in water.

5. (Amended) The method as claimed in claim [2] 3, the step of stripping away the layer of metallic germanium including stripping away the layer of metallic germanium before performing the step of selectively etching the semiconductor substrate.

6. (Amended) The method as claimed in claim [1] 3, the step of depositing a layer of metallic germanium including depositing the layer of metallic germanium having a thickness between approximately 40 nm and approximately 500 nm.

8. (Amended) The method as claimed in claim [1] 3, the step of forming a dielectric layer further including the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and

BUR919990197US1

approximately 3,000 nm over the nitride layer.

11. (Amended) [The] A method [as claimed in claim 10] for fabricating a semiconductor device having a dielectric stack over a major surface thereof, comprising the steps of:

a) depositing a metallic germanium layer over the dielectric stack;

b) patterning the metallic germanium layer to form a germanium hard mask as a top most layer over the dielectric stack, the step further comprising:

i) depositing a photo resist layer over the metallic germanium layer;

ii) exposing and developing the photo resist layer to form a photolithography image; and

iii) etching the metallic germanium layer through the photolithography image;

c) removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask;

d) etching the dielectric stack through the germanium hard mask with the germanium hard mask as a top most layer to form a dielectric hard mask over the major surface of the semiconductor substrate;

e) etching the semiconductor substrate through the dielectric hard mask;

f) forming doped regions in the semiconductor substrate; and

g) forming dielectric and conductive structures over the semiconductor substrate; and further comprising the step of stripping away the metallic germanium layer after the step of etching the dielectric stack and before the step of etching the semiconductor substrate.

BUR919990197US1

wherein the step of stripping away the metallic germanium layer includes the steps of:

oxidizing the metallic germanium layer; and

[rising] rinsing the semiconductor substrate in water.

12. (Amended) The method as claimed in claim [9] 11, wherein the step of depositing a metallic germanium layer includes depositing the metallic germanium layer having a thickness between approximately 40 nm and approximately 500 nm in a chemical vapor deposition process.

14. (Amended) The method as claimed in claim [9] 11, wherein the step of forming a dielectric stack further includes the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm on the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm on the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3000 nm on the nitride layer.

19. (Amended) [The] A method [as claimed in claim 18] for etching a semiconductor wafer, the semiconductor wafer having a dielectric stack over a major surface thereof, the method comprising the steps of:

a) forming a germanium hard mask as a top most layer over the dielectric stack, the step comprising depositing a photo resist layer over the metallic germanium layer;

BUR919990197US1

b) removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask;

c) etching the dielectric stack through the germanium hard mask to form a dielectric hard mask over the major surface of the semiconductor wafer; and

d) etching the semiconductor wafer through the dielectric hard mask; and

wherein the step of forming a germanium hard mask includes the steps of:

depositing a layer of metallic germanium having a thickness equal to or greater than approximately 40nm over the dielectric stack;

patterning the layer of metallic germanium to form the germanium hard mask, and which further includes the steps of:

depositing a photo resist layer over the layer of metallic germanium;

patterning the photo resist layer to form a photolithography mask; and

etching the layer of metallic germanium through the photolithography mask; and

further comprising the step of stripping away the germanium hard mask after etching the dielectric stack and before etching the semiconductor wafer,

wherein the step of stripping away the germanium hard mask includes the steps of:

oxidizing the layer of metallic germanium to convert the layer of metallic germanium into a layer of germanium oxide; and

removing the layer of germanium oxide.

20. (Amended) The method as claimed in claim 19, wherein the step of removing the layer of



BUR919990197US1

germanium oxide includes [rising] rinsing the semiconductor wafer in water.

21. (Amended) The method as claimed in claim [1] 3, wherein the step of patterning the layer of metallic germanium comprises:

depositing a layer of photo resist;

etching the metallic germanium layer through the layer of photo resist; and

removing the layer of photo resist prior to the step of selectively etching the dielectric layer through the germanium hard mask.

26. (Amended) [The] A method [as claimed in claim 25] for etching a semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of germanium over the dielectric layer;

b) depositing a photoresist layer over the germanium layer;

c) exposing and developing the photo resist layer to form a photolithography image;

d) etching the metallic germanium layer through the photolithography image to form a germanium hard mask over the dielectric layer;

e) removing the photoresist layer from over the germanium hard mask;

f) patterning the dielectric layer through the germanium hard a mask after removing the photoresist layer from over the germanium hard mask to form a dielectric hard mask over the semiconductor substrate; and

g) selectively etching the semiconductor substrate through the dielectric hard mask; and further comprising the step of stripping away the germanium hard mask after patterning

BUR919990197US1

the dielectric layer to form the dielectric hard mask, wherein stripping away the layer of germanium comprises:

oxidizing the layer of germanium to form a layer of germanium oxide therefrom; and  
removing the layer of germanium oxide.

28. (Amended) The method as claimed in claim [24] 26, wherein depositing a layer of germanium comprises depositing the layer of germanium having a thickness between approximately 40 nm and approximately 500 nm.

30. (Amended) The method as claimed in claim [24] 26, further comprising forming a dielectric layer by:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

32. (Amended) [The] A method [as claimed in claim 31,] for etching a semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of germanium over the dielectric layer;

b) patterning the layer of germanium to form a germanium hard mask, the step further comprising:

BUR919990197US1

i) depositing a photo resist layer over the metallic germanium layer;

ii) exposing and developing the photo resist layer to form a photolithography image;

iii) etching the metallic germanium layer through the photolithography image; and

iv) removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask;

c) patterning the dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the dielectric layer; and

further comprising the step of stripping away the germanium hard mask after patterning the dielectric layer , the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide

therefrom; and removing the layer of germanium oxide.